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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,560	12/31/2003	David W. Boggs	111079-135918	5692

31817 7590 12/02/2005

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,560	BOGGS ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 19-23* is/are pending in the application.

4a) Of the above claim(s) *9-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 4, 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al., US Patent No. 6,405,431 (Shin).

Regarding claim 1, Shin, in figure 6c, discloses an electronic substrate comprising: a substrate (substrate as shown in figure 6) having two or more electrically conductive inner layer (layer with circuit patterns 62a' and 62a); and one cavity (69a) interconnect cavity extending into, but not through, the substrate, each exposing two of the electrically conductive inner layer (exposing layer with circuit patterns 62a' and 62a).

Regarding claim 2, Shin further discloses one electrically conductive surface layer (layer with circuit pattern 64), wherein the interconnect cavity extends from the electrically conductive surface layer (layer with circuit pattern 64), to the electrically conductive inner layer (layer with circuit patterns 62a).

Regarding claim 3, Shin further discloses the interconnect cavity comprises a base (base of the cavity 69a on 62a) adjacent to the electrically conductive inner layer (layer with circuit pattern 62a), the base comprising a layer of electrically conductive material (base of the cavity 69a, formed by part of layer 64).

Regarding claim 4, Shin further discloses the interconnect cavity comprises a base (base of the cavity 69a) adjacent to the electrically conductive inner layer (62a), wherein the interconnect cavity defines a wall (wall of cavity 69a) interconnected with the base adjacent electrically conductive inner layer (62a).

Regarding claim 5, Shin further discloses the interconnect cavity comprises a base (base of the cavity 69a) adjacent to and electrically interconnected with the conductive inner layer (62a), the interconnect cavity extending from a surface layer (64) defines a wall (wall of cavity 69a) interconnected with the base adjacent electrically conductive inner layer (62a) and the surface layer (64).

Regarding claim 6, Shin further discloses the interconnect cavity is adapted to receive and interconnect with electrically conductive interconnect material (see figure).

Regarding claim 7, Shin further discloses the interconnect cavities are positioned to correspond land pads of a surface mount technology electrical component (as the circuit board is for mounting components, column 2, line 13-16).

Regarding claim 8, Shin further discloses at least one of the interconnect cavities comprises a base (base of the cavity 69a) adjacent to the electrically conductive inner layer (62a) and an opening at a surface of the substrate, the base having a smaller diameter than the opening (base of the cavity 69a smaller than the opening, see figure 6c).

4. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin, as applied to claims 1-7 above, and further in view of Ho et al., US Patent No. 6,717,264.

Regarding claim 19, Shin, figure 6, discloses an electronic device comprising: a substrate (substrate as shown in figure 6) including two electrically conductive inner layers (layers with circuit pattern 62' and 62a); and one interconnect cavity (69a) extending into a surface of, but no through the substrate exposing two electrically conductive inner layer (layers with circuit pattern 62' and 62a).

Shin does not disclose an electronic component, having component interconnects, mounted on the substrate. However, Shin in the background states that the substrate structure is for mounting the components, column 1, line 11-30. Further, it is known in the art to use the substrate for mounting the component and wherein the substrate facilitates the interconnection of the devices. Also, component mounted on a substrate can be seen by opening of any electronic device such as computer etc. Ho, in figure 4F, discloses a component (300) with interconnect, mounted on the substrate for desired interconnection for the functioning of the device.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to mount a component on the substrate of Shin, in order to facilitate interconnection between the component for the functionality of the devices, as taught by Ho.

Regarding claim 20,the modified assembly of Shin further discloses the substrate further comprises one electrically conductive surface layer (64), wherein one of the interconnect cavity (69a) extends from at least one of the surface layer to the electrically conductive inner layer (62a').

Regarding claim 21, the modified assembly of Shin further discloses at least one of the interconnect cavities comprises a base (base of the cavity 69a) adjacent to the electrically conductive inner layer (62a), the base comprising a layer of electrically conductive material (part of 64 in cavity 69a).

Regarding claim 22, the modified assembly of Shin further discloses at least one of the interconnect cavities comprises a base (base of the cavity 69a) adjacent to the electrically conductive inner layer (62a), wherein the interconnect cavity defines a wall (wall of cavity 69a) interconnected with the base adjacent conductive inner layer (62a).

Regarding claim 23, the modified assembly of Shin further discloses the electronic component is a microelectronic die (300, Ho).

Response to Arguments

5. Applicant's arguments with respect to claims 1-8 and 19-23 have been considered but are moot in view of the new ground(s) of rejection.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yasuda et al., US Patent No. 5,347,712, in figure 11, discloses substrate with a cavity, not passing through the substrate and exposing two inner layers.

Burgess, US Patent No. 6,631,558, in figure 26, disclose a structure with cavity (113') exposing tow internal layers.

Takada et al., US Patent No. 6,590,165, in figure 27, discloses a structure with cavity (402) exposing two inner layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
November 27, 2005